REMARKS

A total of 71 claims remain in the present application. The foregoing amendments are presented in response to the Office Action mailed December 29, 2004, wherefore reconsideration of this application is requested.

By way of the above-noted amendments, claims 1, 11, 22, 23, 46, 54, 55, 66, 74, 75 and 85 have been amended to more clearly define features of the present invention. In particular, independent claim 1 has been amended to define that the egress interface has "a respective plurality of logical egress network ports", and that, within the egress interface, the data traffic is forwarded "to one or more of the respective plurality of logical egress network ports based on the parameter". Similar amendment have been effected in independent claims 23, 55 and 74. Dependent claims 11, 22, 23, 46, 66, 75 and 85 have been amended to reflect the revisions effected in claims 1, 23, 55 and 74. Claims 47-53 and 67-73 have been cancelled.

In preparing the above-noted amendments, careful attention was paid to ensure that no new subject matter has been introduced. In particular, support for amended claims 1, 23, 55 and 74 is found in figures 2 and 4 and in the accompanying description in the originally filed specification.

Referring now to the text of the Office Action:

- claim 71 have been objected to of improperly depending from itself; and
- claims 1-85 stand rejected under 35 U.S.C. § 102(e), as being unpatentable over the teaching of United States Patent Application No. 2002/0196796 (Ambe et al.).

The Examiner's claim rejections are believed to be traversed by the above-noted claim amendments, and further in view of the following discussion.

United States Patent Application No. 2002/0196796 (Ambe et al.) filter processor architecture for a network device, in which "an incoming packet is received from a port and the incoming packet is inspected and packet fields are extracted. The incoming packet is classified

based on the extracted packet fields and action instructions are generated. The incoming packet is then modified based on the action instructions. Further, the inspection and extraction includes applying inspection mask windows to any portion of the incoming packet to extract programmable packet fields." (Abstract)

According to Ambe et al, incoming data packets are processed by an ingress submodule 14a (FIG. 8), which performs a table lookup to find a destination address, and then slices the packet into 64 byte cells (paragraph 106)

> All incoming packet processing occurs in ingress submodule 14, and features such as the fast filtering processor, layer two (L2) and layer three (L3) lookups, layer two learning, both self-initiated and CPU 52 initiated, layer two table management, layer two switching, packet slicing, and channel dispatching occurs in ingress submodule 14. After lookups, fast filter processing, and slicing into cells, as noted above and as will be discussed below, the packet is placed from ingress submodule 14 into dispatch unit 18, and then placed onto CPS channel 80 and memory management is handled by PMMU 70. ... Once the cells or cellularized packets are placed onto the CPS channel 80, the ingress submodule is finished with the packet. The ingress is not involved with dynamic memory allocation, or the specific path the cells will take toward the destination. Egress submodule 16, illustrated in FIG. 8 as submodule 16a of EPIC 20a, monitors CPS channel 80 and continuously looks for cells destined for a port of that particular EPIC 20. When the PMMU 70 receives a signal that an egress associated with a destination of a packet in memory is ready to receive cells, PMMU 70 pulls the cells associated with the packet out of the memory, as will be discussed below, and places the cells on CPS channel 80, destined for the appropriate egress submodule. ..." (Paragraph 107)

Thus it will be seen that, in the system of Ambe et al., The ingress submodule 14 performs all of the input processing, including " layer two (L2) and layer three (L3) lookups, layer two learning, ... layer two table management, layer two switching, packet slicing, and

channel dispatching". Each egress submodule 16a continuously monitors the CPS channel 80 to look for cells destined for a port of that particular EPIC 20. Cells destined for that port are received from the PMMU 70, assembled back into data packets, and then passed to the destination port.

It will be noted that, in the system of Ambe et al, the destination address of each cell is determined by the ingress submodule 14a. The egress submodule merely looks for cells destined for a port on its EPIC 20, and uses the cell address to forward each cell to the appropriate egress port. Forwarding of cells to more than one egress port necessarily involves replication of the cells for each destination port, and assignment of respective different addresses to each (replicated) set of cells, so that each set of cells will be "seen" by the respective egress submodules that service the destination ports. Since all cell addressing is performed by ingress submodule 14a, any such cell replication (and associated addressing) would also have to be performed by the ingress submodule 14a. Ambe et al. do not teach or suggest that the ingress submodule 14a are capable of performing any such function, and even if such a modification were made, the resulting structure would merely be representative of the prior art described in the background to the present invention.

In contrast, the present invention provides a system and methods in which the cell addressing and replication functions are divided between the ingress and egress interfaces. Thus, the present invention provides an egress interface which has a respective plurality of logical egress ports, and which is adapted to forward data traffic to any one or more of the respective logical egress ports. As such, the egress interface is capable of replicating received cells/packets, as needed, in order to route the cells to the required logical egress ports. Ambe et al. do not teach or suggest any equivalent to this functionality. In fact, Ambe et al teach directly away from the present invention, by requiring that all cell addressing is performed in the ingress submodule (interface).

In light of the foregoing, it is respectfully submitted that the presently claimed invention is clearly distinguishable over the teaching of the cited reference, and is therefore

patentable. Thus it is believed that the present application is in condition for allowance, and early action in that respect is courteously solicited.

If any extension of time under 37 C.F.R. § 1.136 is required to obtain entry of this response, such extension is hereby respectfully requested. If there are any fees due under 37 C.F.R. §§ 1.16 or 1.17 which are not enclosed herewith, including any fees required for an extension of time under 37 C.F.R. § 1.136, please charge such fees to our Deposit Account No. 19-5113.

Respectfully submitted,

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